ABSTRACT OF THE DISCLOSURE

A PMOS device can be designed and manufactured in accordance with the invention to locate its drain junction breakdown point and maximum impact ionization point to reduce or eliminate drain breakdown voltage walk-in. In some embodiments, the drain junction breakdown point and maximum impact ionization point are located sufficiently far from the gate that the device exhibits no significant drain breakdown voltage walk-in. The device can be a high voltage power transistor having an extended drain region including a P-type lightly doped drain (P-LDD) implant, with drain junction breakdown and maximum impact ionization points appropriately located by controlling the implant dose employed to produce the P-LDD implant. Other aspects of the invention are methods for designing a PMOS device including by determining relative locations of the gate and at least one of the drain junction breakdown and maximum impact ionization points to reduce drain breakdown voltage walk-in, and methods for manufacturing integrated circuits including any embodiment of the PMOS device of the invention.